

ABSTRACT OF THE DISCLOSURE

There is provided apparatus for processing data, said apparatus comprising:
a processor operable in a plurality of modes and either a secure domain or a
5 non-secure domain including:
at least one secure mode being a mode in said secure domain; and
at least one non-secure mode being a mode in said non-secure domain;
wherein
when said processor is executing a program in a secure mode said program has
10 access to secure data which is not accessible when said processor is operating in a
non-secure mode;
said processor includes a non-secure translation table base address register
operable in said non-secure domain to indicate a region of memory storing non-secure
domain memory mapping data defining how virtual addresses are translated to
15 physical addresses within said non-secure domain; and
said processor includes a secure translation table base address register
operable in said secure domain to indicate a region of memory storing secure domain
memory mapping data defining how virtual addresses are translated to physical
addresses within said secure domain.

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[Figure 1]